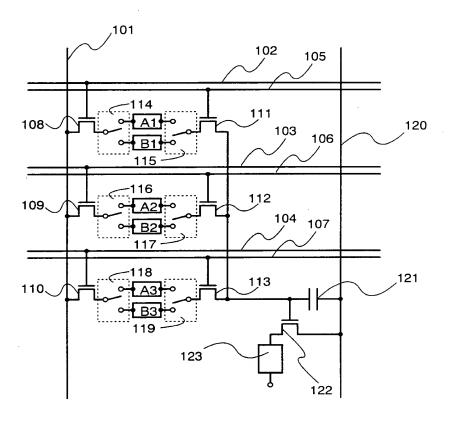
Fig. 1



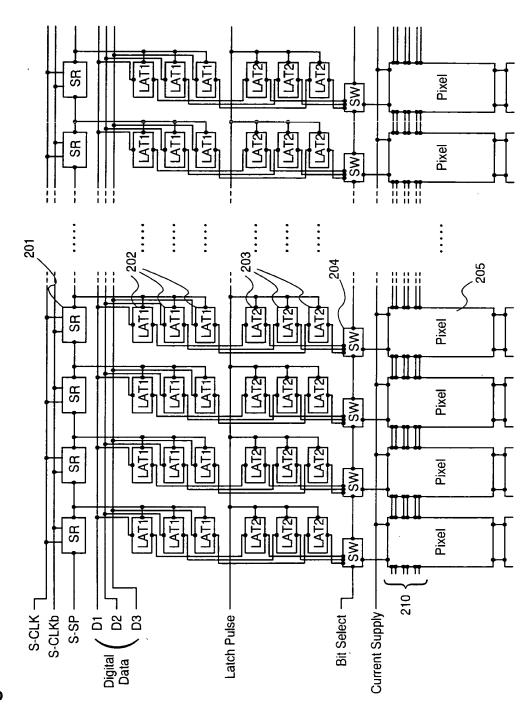
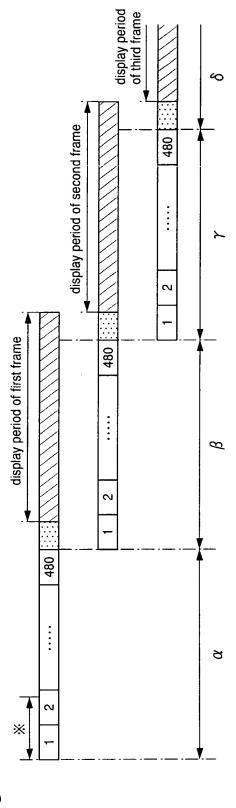
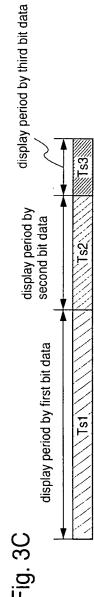


Fig. 2

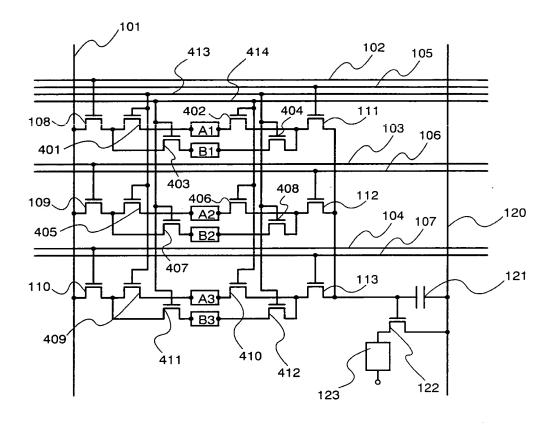
Fig. 3A



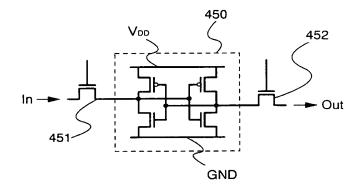
dot data sampling period of next column writing period to memory latch data transfer period 640 dod data sampling period Fig. 3B



Flg. 4A



Flg. 4B



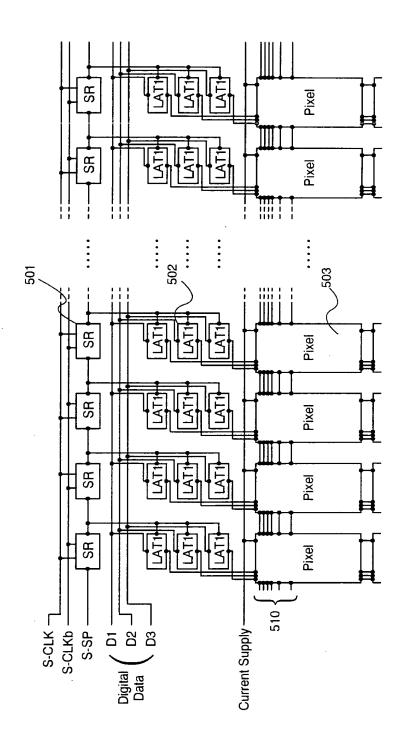


Fig. 5

Fig. 6

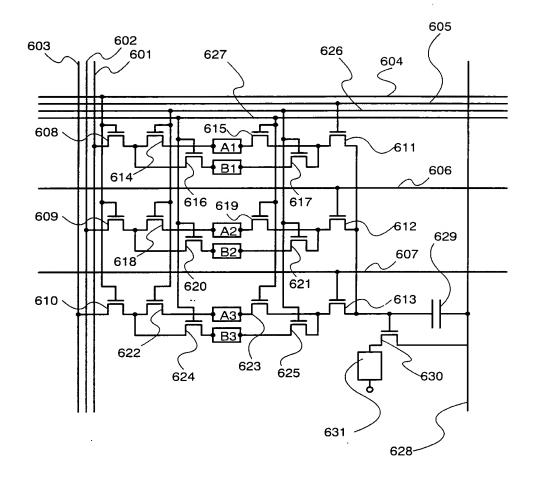
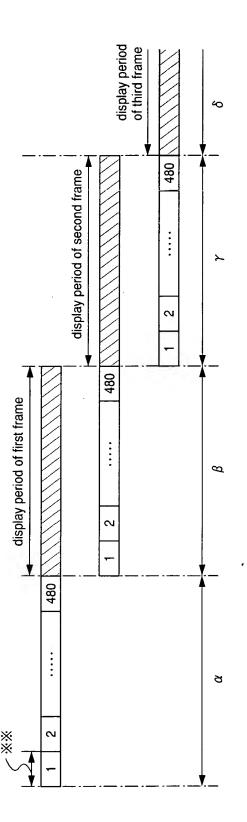
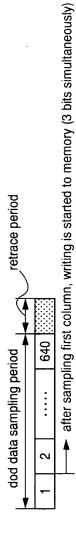


Fig. 7A





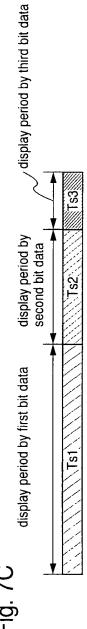


Fig. 8

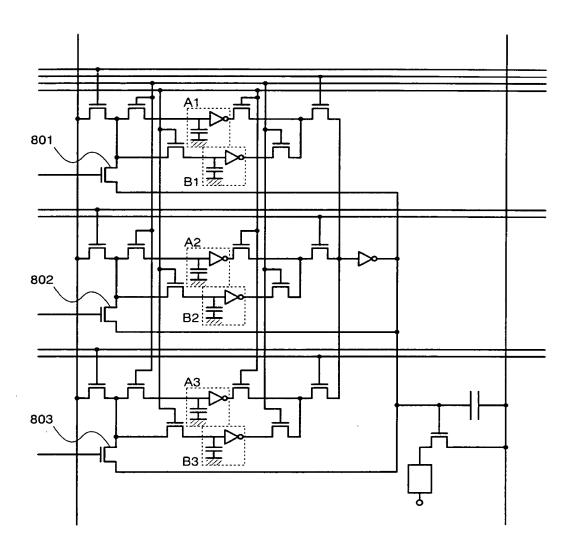
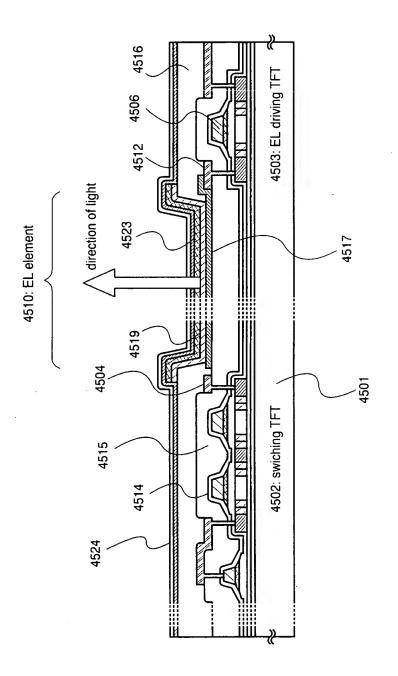
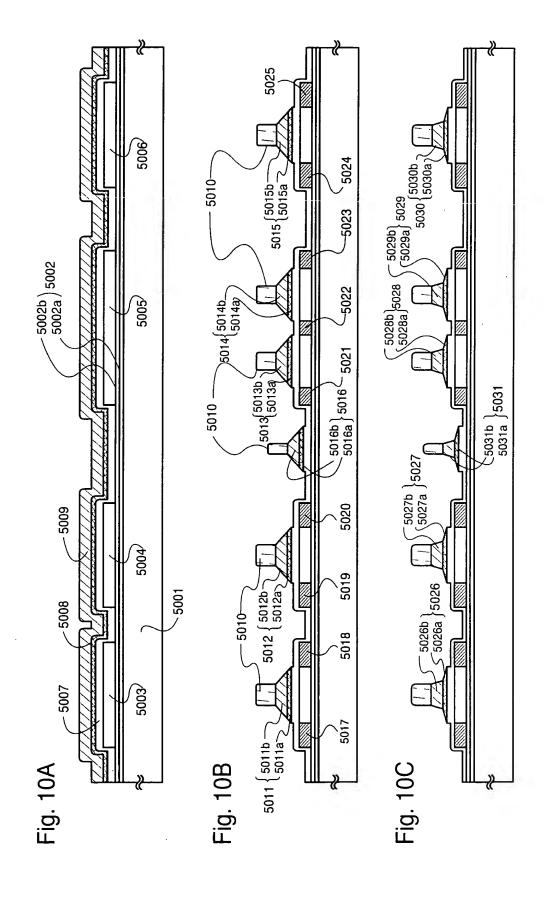
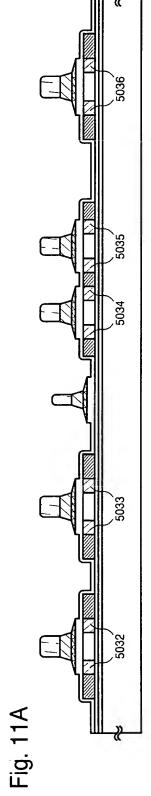
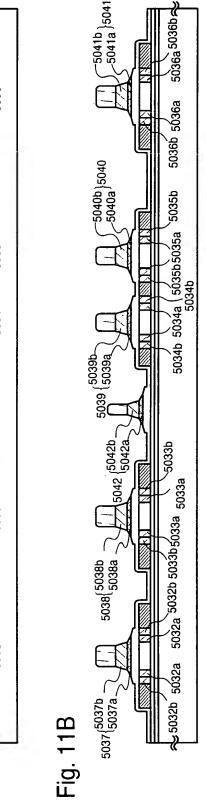


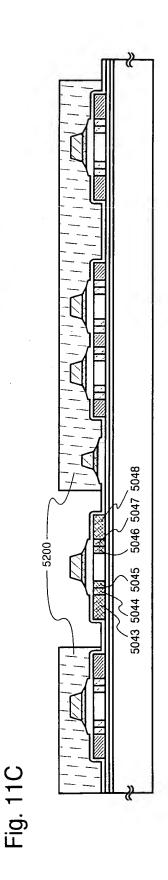
Fig. 9











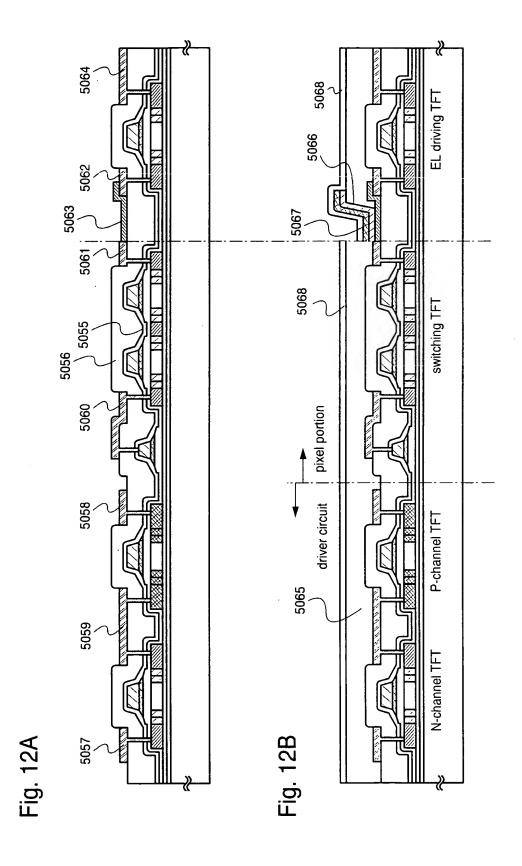
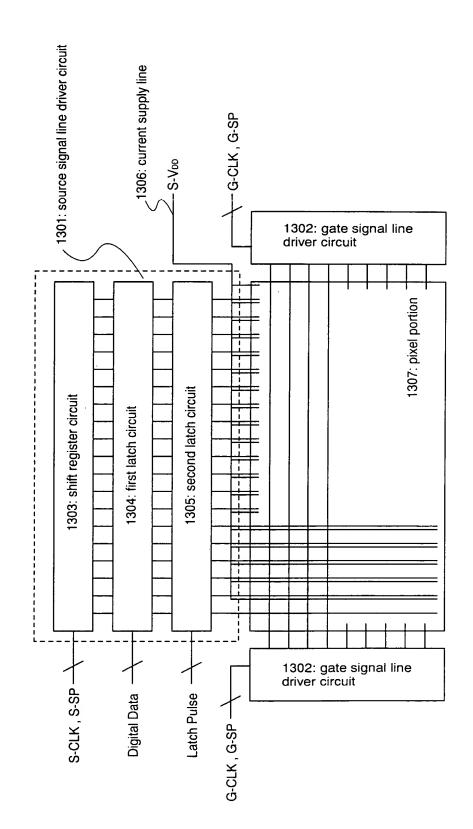
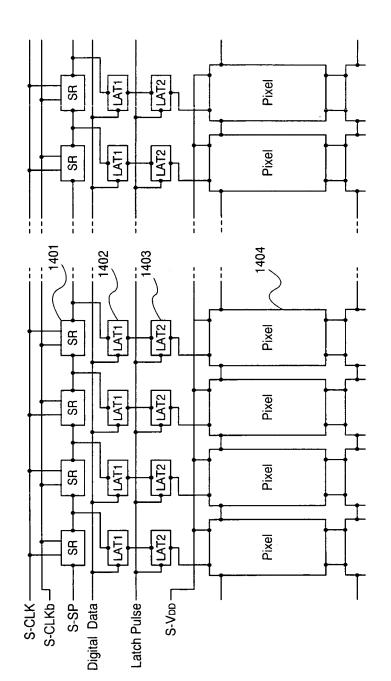
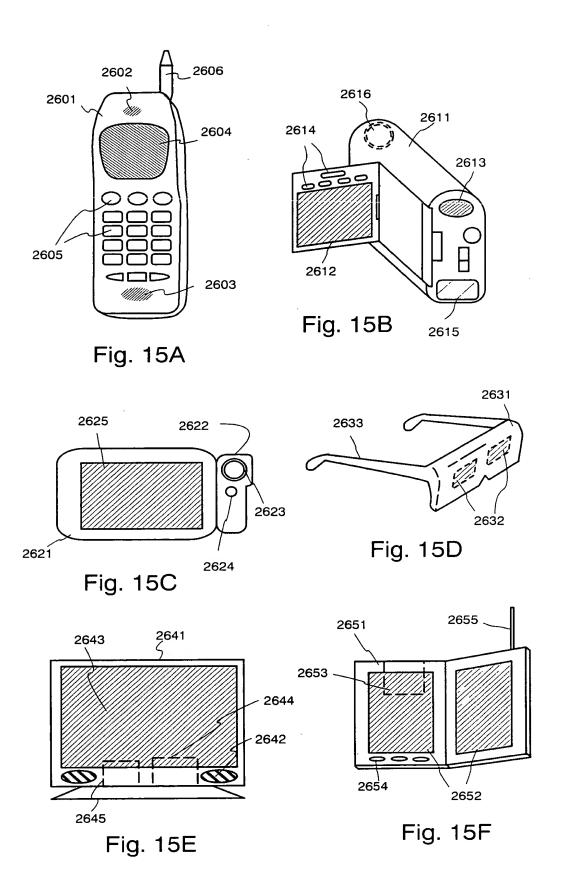


Fig. 13



Flg. 14





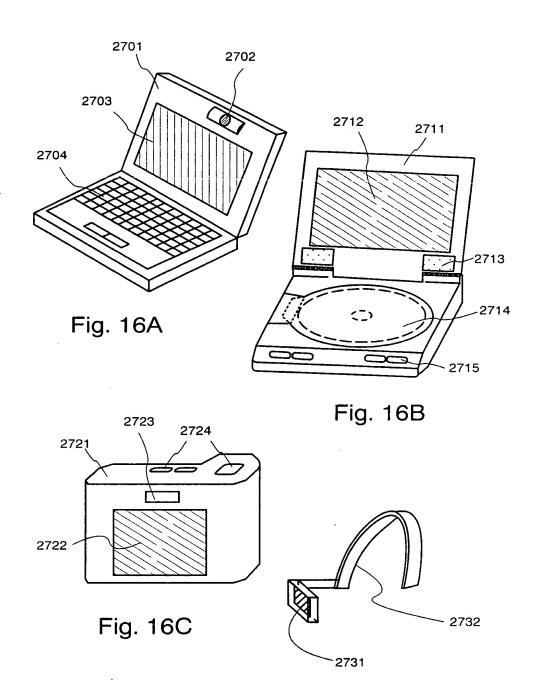


Fig. 16D

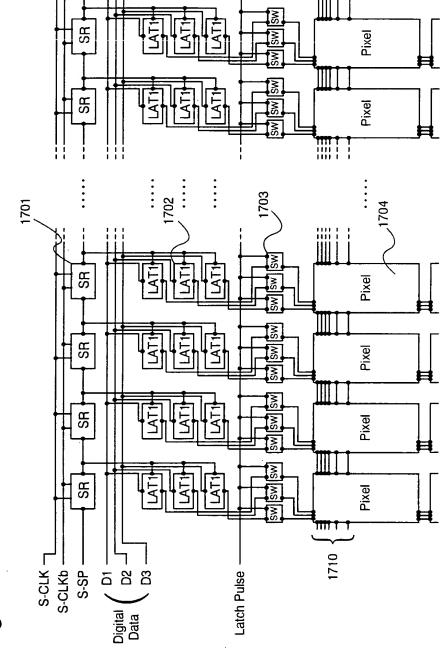


Fig. 17

Fig. 18A

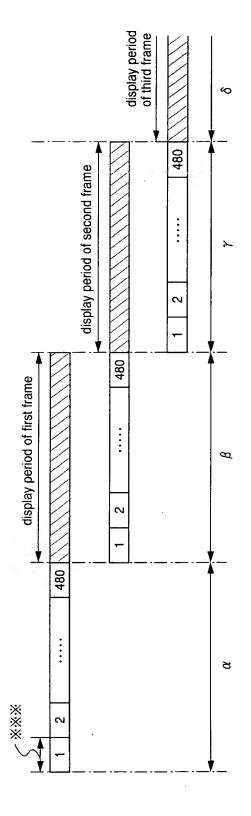


Fig. 18B

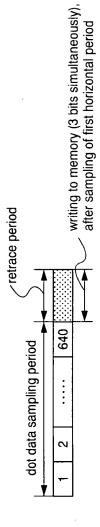


Fig. 18C

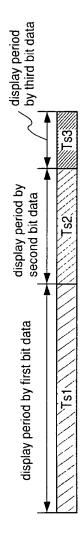


Fig. 19A

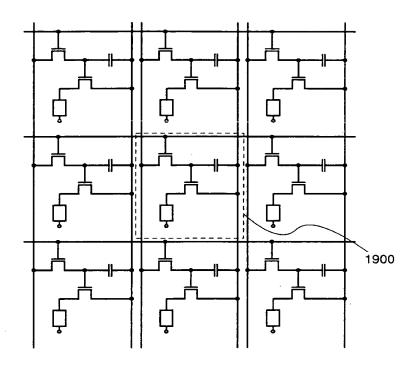


Fig. 19B

1905

1906

1909

1902

1908

Fig. 20A

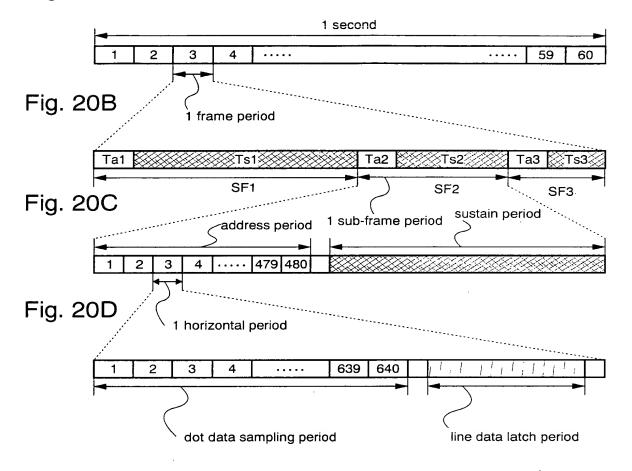


Fig. 21

